CLAIM AMENDMENTS

IN THE CLAIMS

This listing of the claims will replace all prior versions, and listing, of claims in the application or previous response to office action:

1. **(Currently Amended)** A method for synchronizing a plurality of bus systems, said method comprising:

transmitting synchronization signals from a transmission unit to an associated reception unit **said associated reception unit supplying synchronization signals to a phase regulator in a phase locked loop having a clock transmitter**, where each bus system has at least one transmission unit and at least one associated reception unit; said transmission unit using a central clock to generate said synchronization signals autonomously for cyclic transmission to said associated reception unit, wherein said central clock is prescribed for each of said transmission units in a bus system; ~~and~~

upon receipt of said synchronization signals, said phase regulator ascertains instantaneous phase errors and readjusts the clock transmitter such that said clock transmitter outputs a nominal number of clock signals between two synchronization signals, wherein said nominal number of clock signals is prescribed as said central clock for a transmission unit in second another bus system; and

transmitting data between said synchronized transmission unit and associated reception unit.

2. (Previously Presented) The method of claim 1, wherein said reception unit in a bus system supplies the synchronization signals to a phase regulator in a phase locked loop having a clock transmitter, and upon receipt of said synchronization signals said phase regulator ascertains instantaneous phase errors and readjusts the clock transmitter such that said clock transmitter outputs a nominal number of clock signals between two synchronization signals, wherein said nominal number of clock signals is prescribed for all transmission units in said bus systems as said central clock.

3. **(Canceled)**

4. **(Currently Amended)** The method of claim ~~2~~ 1 or ~~3~~ 2, wherein said phase regulator integrates the instantaneous phase errors to form an integration value, and wherein said integration value is corrected to form an integration fraction, with said integration fraction being less than one.

5. (Previously Presented) The method of claim 1, wherein a clock division is effected before said transmission unit is driven using a central clock.

6. (Previously Presented) The method of claim 1, wherein frequency multiplication is effected within the phase locked loop before a transmission unit is driven using a central clock.

7. **(Currently Amended)** The method of claim ~~2~~ 1 or ~~3~~ 2, wherein a message end of a clock message represents a respective clock instant, wherein said central clock generated by said phase locked loop is prescribed so that it is advanced by a delay time of a received clock message.

8. **(Currently Amended)** The method of claim ~~2~~ 1 or ~~3~~ 2, wherein a plurality of phase locked loops in a plurality of bus systems are cascaded.

9. (Previously Presented) The method of claim 8, wherein said frequency response of each of said phase locked loops has a gain of less than or equal to unity.

10. **(Canceled)**

11. (Previously Presented) The method of claim 1, wherein said central clock is a common clock for all bus systems.

12. (Previously Presented) A method for synchronizing a plurality of bus systems, said method comprising:

transmitting synchronization signals from a transmission unit to an associated reception unit, where each bus system has at least one transmission unit and at least one associated reception unit; and

said transmission unit using a central clock to generate said synchronization signals autonomously for cyclic transmission to said associated reception unit, wherein said central clock is prescribed for each of said transmission units in a bus system;

wherein said reception unit in a bus system supplies the synchronization signals to a phase regulator in a phase locked loop having a clock transmitter, and upon receipt of said synchronization signals said phase regulator ascertains instantaneous phase errors and readjusts the clock transmitter such that said clock transmitter outputs a nominal number of clock signals between two synchronization signals, wherein said nominal number of clock signals is prescribed for all transmission units in said bus systems as said central clock.

13. (Previously Presented) The method of claim 12, wherein said phase regulator integrates the instantaneous phase errors to form an integration value, and wherein said integration value is corrected to form an integration fraction, with said integration fraction being less than one.

14. (Previously Presented) The method of claim 12, wherein a clock division is effected before said transmission unit is driven using a central clock.

15. (Previously Presented) The method of claim 12, wherein frequency multiplication is effected within the phase locked loop before a transmission unit is driven using a central clock.

16. (Previously Presented) The method of claim 12, wherein a message end of a clock message represents a respective clock instant, wherein said central clock generated by said phase locked loop is prescribed so that it is advanced by a delay time of a received clock message.

17. (Previously Presented) The method of claim 12, wherein a plurality of phase locked loops in a plurality of bus systems are cascaded.

18. (Previously Presented) The method of claim 17, wherein said frequency response of each of said phase locked loops has a gain of less than or equal to unity.

19. (Previously Presented) A method for synchronizing a plurality of bus systems, said method comprising:

transmitting synchronization signals from a transmission unit to an associated reception unit, where each bus system has at least one transmission unit and at least one associated reception unit;

said transmission unit using a central clock to generate said synchronization signals autonomously for cyclic transmission to said associated reception unit, wherein said central clock is prescribed for each of said transmission units in a bus system; and

a reception unit in a first bus system supplying synchronization signals to a phase regulator in a phase locked loop having a clock transmitter; upon receipt of said synchronization signals, said phase regulator ascertains instantaneous phase errors and readjusts the clock transmitter such that said clock transmitter outputs a nominal number of clock signals between two synchronization signals, wherein said nominal number of clock signals is prescribed as said central clock for a transmission unit in second another bus system.

20. (Previously Presented) The method of claim 19, wherein said phase regulator integrates the instantaneous phase errors to form an integration value, and wherein said integration value is corrected to form an integration fraction, with said integration fraction being less than one.